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WHAT IS CLAIMED IS:

1. A semiconductor packaging substrate, comprising:

a laminated circuit structure having a first surface and a second surface, the laminated circuit structure comprising:

a plurality of patterned internal metal layers stacked up;

a plurality of internal insulation layers, wherein each of the internal insulation layers is interposed between two adjacent internal metal layers; and

at least one contact via formed through the internal metal layers and the internal insulation layers, such that the internal metal layers are electrically connected to one another;

a build-up circuit structure on the first surface and the second surface of the laminated circuit, the build-up circuit structure comprising:

a first external insulation layer having at least one first via and a second external insulation layer having at least one second via respectively arranged on the first surface and the second surface of the laminated circuit;

; and

a patterned first external metal layer located on the first external insulation layer and a patterned second external metal layer located on the second external insulation layer, wherein the first external metal layer and the second external metal layer are electrically connected to the internal metal layers of the laminated circuit by the first and the second vias, respectively, and wherein the first external metal layer has a plurality of firstexternally

exposed areas and the second external metal layer has a plurality of second externally exposed areas.

2. The substrate of claim 1, further comprising a first solder mask that covers the first external insulation layer and the first external metal layer, and exposes the the first externally exposed areas.

3. The substrate of claim 1, further comprising a second solder mask that covers the second external insulation layer and the second external metal layer, and exposes the second externally exposed areas.

4. The substrate of claim 1, wherein the substrate is used as a flip-chip ball grid array packaging substrate.

5. The substrate of claim 1, wherein the first externally exposed areas are used as bump pads and the second externally exposed areasare used as ball pads.

6. A process for forming a semiconductor packaging substrate, comprising:

forming a laminated circuit having a first surface and a second surface opposite to the first surface, wherein the laminated circuit has a plurality of patterned internal metal layers stacked up, and has a plurality of internal insulation layers each of which is interposed between two adjacent internal metal layers;

forming at least one contact via through the internal metal layers and the internal insulation layers, such that the internal metal layers electrically connect to one another;

forming a first external insulation layer and a second external insulation layer respectively on the first surface and the second surface of the laminated circuit, wherein the

first external insulation layer has at least one first opening and the external second insulation layer has at least one second opening;

forming a first via in each of the first opening and a second via in each of the second opening;

forming a first external metal layer on the first external insulation layer and a second external metal layer on the second external insulation layer, wherein the first and second external metal layer are electrically connected to the internal metal layers of the laminated circuit respectively through the first and second vias, and wherein the first external metal layer has a plurality of first externally exposed areas and the second external metal layer has a plurality of second externally exposed areas.

7. The process of claim 6, wherein the forming the contact via includes mechanically drilling and plating on the laminated circuit.

8. The process of claim 6, wherein the forming the first and the second vias includes non-mechanically drilling and plating on the first and second external insulation layers, respectively.

9. The process of claim 7, wherein the non-mechanically drill is selected from a group consisting of photo-via forming, laser ablating and plasma etching.

10. The process of claim 6, further comprising a step of forming a first solder mask on the first external metal layer to cover the first external insulation layer and expose the first externally exposed areas, after forming the first external metal layer.

11. The process of claim 6, further comprising a step of forming a second solder mask on the second external metal layer to cover the second external insulation layer and expose the second externally exposed areas, after forming the second external metal layer.

12. The process of claim 6, wherein the semiconductor packaging substrate is a flip-chip ball grid array packaging substrate.

13. The process of claim 6, wherein forming the internal metal layers of the laminated circuit includes forming and patterning copper foils.

14. A semiconductor packaging substrate, comprising:

a first, second, third, fourth, fifth, and sixth patterned metal layers sequentially stacked up, wherein the first metal layer has a plurality of power/ground bump pads, a plurality of first signal bump pads and a plurality of second signal bump pads, and wherein the first signal bump pads surround the power/ground bump pads and are surrounded by the second signal bump pads, and wherein the sixth metal layer has a plurality of ball pads;

a plurality of inner insulation layers, located between the second and third metal layers, between the third and fourth metal layers, and between the fourth and fifth metal layers; and

at least one contact via formed through the insulation layers and the second, the third, the fourth, and the fifth metal layers, such that the second, the third, the fourth, and the fifth metal layers are electrically connected to one another;

a first external insulation layer and a second external insulation layer arranged between the first and second metal layers and between the fifth and the sixth metal layers, respectively; and

at least one first via formed through the first external insulation layer i and at least one second via formed through the second external insulation layer, thereby the first metal layer being electrically connected to the second metal layer through the first via, and the sixth metal layer being electrically connected to the fifth metal layer through the second via;

wherein the first signal bump pads are routed to the sixth metal layer and then fanned out to the corresponding ball pads, the second signal bump pads arefanned out on the first metal layer and then routed to the corresponding ball pads , and the power/ground bump pads are routed to the third and fourth metal layers and then fanned out to the corresponding ball pads.

15. The substrate of claim 14, further comprising a first solder mask arranged on the first external metal layer to cover the first external insulation layer and expose the power/ground bump pads, the first signal bump pads and the second signal bump pads.

16. The substrate of claim 14, further comprising a second solder mask arranged the sixth metal layer to cover the second external insulation layer and expose the ball pads.

17. The substrate of claim 14, wherein the substrate is used as a flip-chip ball grid array packaging substrate.